Amendments to the Specification:

Please replace the paragraph beginning on page 6, line 31, with the following amended paragraph:

Fig. 1 depicts a tracking data cell 10, according to the invention. The tracking data cell 10 comprises a pair of track and hold circuits 1, 1' coupled to a first multiplexer 5. A clock signal H+, H- is inputted substantially in anti-phase in the respective track and hold circuits 1, 1' for determining receipt of a data signal D+, D- having a rate. The track and hold circuits 1, 1' provide an output signal O having a substantially half rate. In high-speed decision circuits, which work at full-rate of an input signal as e.g. flip-flops, latches the most difficult function is memorizing. The decision circuits have to decide at full speed and to track the input data signal sufficiently fast such that the setup and hold conditions of the decision circuits e.g. latches, flip-flops are not violated. Hence, in these conditions, a track and hold circuit helps, it holds the input data and does not to take a decision whether the input data is at a low or at a high level. Here the output signal O of the multiplexer 5 is substantially equal with the input signal D+, D-. This circuit has the advantage that the outputs of the track and hold circuits 1, 1' may be used to generate a half-rate version of the input signal by adding the two track and hold circuits 1, 1' clocked in anti-phase by the ~~selock~~ clock signals H+, H-.